WHAT IS CLAIMED IS:

1. A magnetic random access memory device comprising:

a magnetoresistive element which stores data in accordance with a size of a resistance value between first and second magnetic layers which varies in accordance with magnetization arrangement states of the first and second magnetic layers, a non-magnetic layer being sandwiched between the first and second magnetic layers;

a write wiring which is arranged in the vicinity of the first magnetic layer, generates an induced magnetic flux when a write current is caused to flow therethrough, and writes data in the magnetoresistive element by changing a magnetization direction in the first magnetic layer when the induced magnetic flux is applied to the magnetoresistive element; and

a third magnetic layer which is provided so as to cover at least a peripheral surface including a first part of the write wiring opposed to the first magnetic layer of peripheral surfaces of the write wiring,

wherein the first magnetic layer has a crystal magnetic anisotropy exceeding 10^4 erg/cc and the first magnetic layer is exchange-coupled with the third magnetic layer, and

a sum of a magnetic volume of a second part of the third magnetic layer opposed to the first part of the

write wiring and that of the first magnetic layer is smaller than a magnetic volume of the third magnetic layer at parts other than the second part.

2. A magnetic random access memory device according to claim 1, further comprising a ruthenium film provided between the first magnetic layer and the second part of the third magnetic layer opposed to the first magnetic layer.

3. A magnetic random access memory device according to claim 1, wherein a ratio of a sum of a magnetic volume of the second part of the third magnetic layer and that of the first magnetic layer relative to a magnetic volume of the third magnetic layer at parts other than the second part is not more than 0.9.

4. A magnetic random access memory device according to claim 3, wherein a ratio of a sum of a magnetic volume of the second part of the third magnetic layer and that of the first magnetic layer relative to a magnetic volume of the third magnetic layer at parts other than the second part is not more than 0.3.

5. A magnetic random access memory device according to claim 1, wherein the exchange coupling is of a ferro type.

6. A magnetic random access memory device according to claim 1, wherein the exchange coupling is

of an anti-ferro type.

7. A magnetic random access memory device according to claim 1, wherein the exchange coupling is substantially 90-degree coupling.

8. A magnetic random access memory device according to claim 1, wherein the third magnetic layer has a larger magnetic permeability than that of the first magnetic layer.

9. A magnetic random access memory device according to claim 1, wherein the third magnetic layer has a higher saturation magnetic flux density than that of the first magnetic layer.

10. A magnetic random access memory device according to claim 1, wherein a thickness of the second part of the third magnetic layer is smaller than a thickness of any other part of the third magnetic layer.

11. A magnetic random access memory device according to claim 1, wherein the first magnetic layer is composed of a magnetic layer having a multilayer structure.

12. A magnetic random access memory device according to claim 1, further comprising a write cell selection transistor which is connected to the write wiring, and heats the first magnetic layer by using the write current caused to flow through the write wiring at the time of writing data into the magnetoresistive

element, thereby writing the data.

13. A magnetic random access memory device comprising:

a magnetoresistive element which stores data in accordance with a size of a resistance value between first and second magnetic layers which varies in response to magnetization states of the first and second magnetic layers, a non-magnetic layer being sandwiched between the first and second magnetic layers, the first magnetic layer having a crystal magnetic anisotropy exceeding 10^4 erg/cc;

a write wiring which is arranged in the vicinity of the first magnetic layer, generates an inducted magnetic flux when a write current is caused to flow therethrough, and writes data into the magnetoresistive element by changing a magnetization direction in the first magnetic layer when the induced magnetic flux is applied to the magnetoresistive element; and

a third magnetic layer which is provided so as to cover a peripheral surface of the write wiring opposed to the first magnetic layer, and has a concave portion in which at least the first magnetic layer of the magnetoresistive element is arranged.

14. A magnetic random access memory device according to claim 13, further comprising a ruthenium film which is provided between the first magnetic layer and a bottom surface of the concave portion of the

third magnetic layer opposed to the first magnetic layer, an intensity of exchange coupling between of the first magnetic layer and the third magnetic layer being controlled by a thickness of the ruthenium film.

ABSTRACT OF THE DISCLOSURE

A recording layer of an MTJ element is constituted by using a high crystal magnetic anisotropic material. A write wiring used to write data into the MTJ element is covered with a magnetic layer, and the write wiring and the magnetic layer are exchange-coupled with each other. A sum of a magnetic volume of the magnetic layer at a part opposed to the recording layer of the MTJ element and that of the recording layer is set smaller than a magnetic volume of the magnetic layer at any other part.

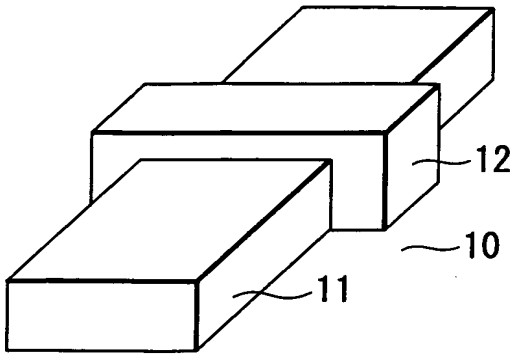


FIG. 1 (PRIOR ART)

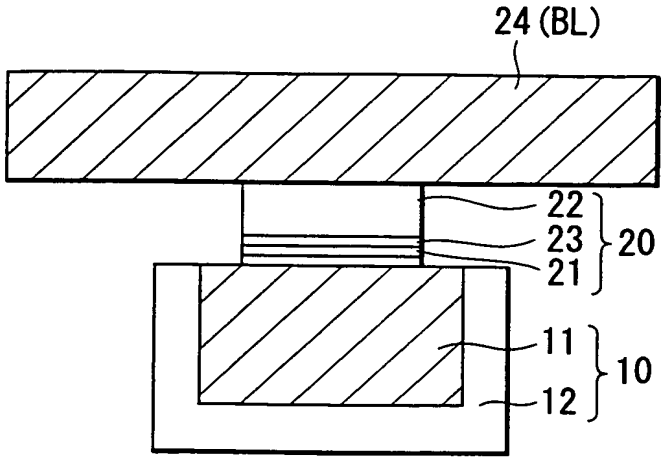


FIG. 3 (PRIOR ART)

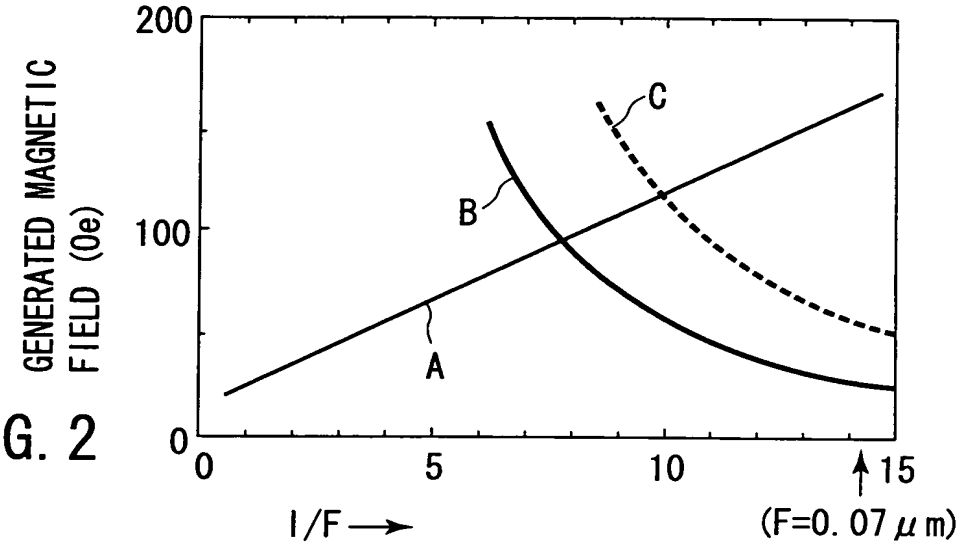


FIG. 2

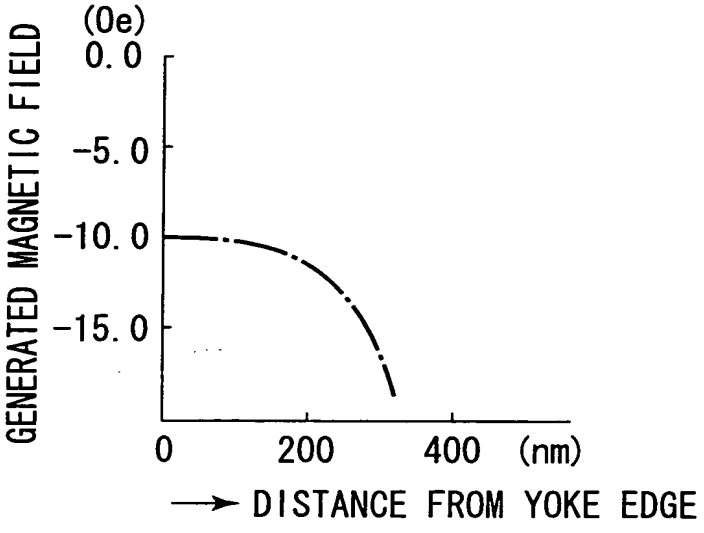


FIG. 4

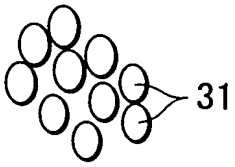


FIG. 5

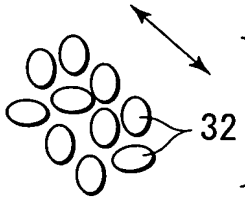
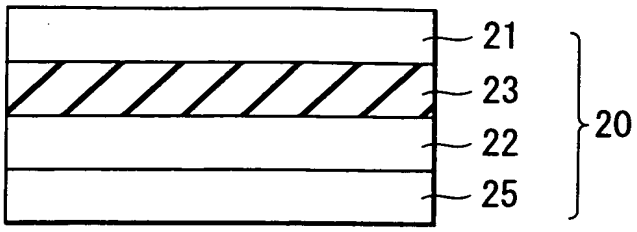


FIG. 6

FIG. 7



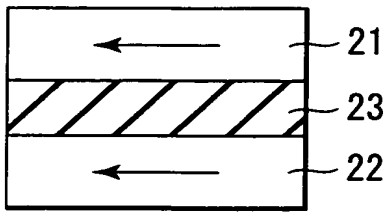


FIG. 8A

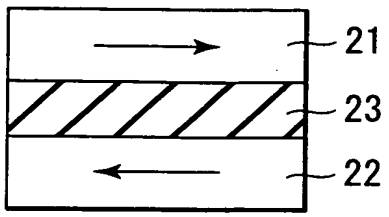


FIG. 8B

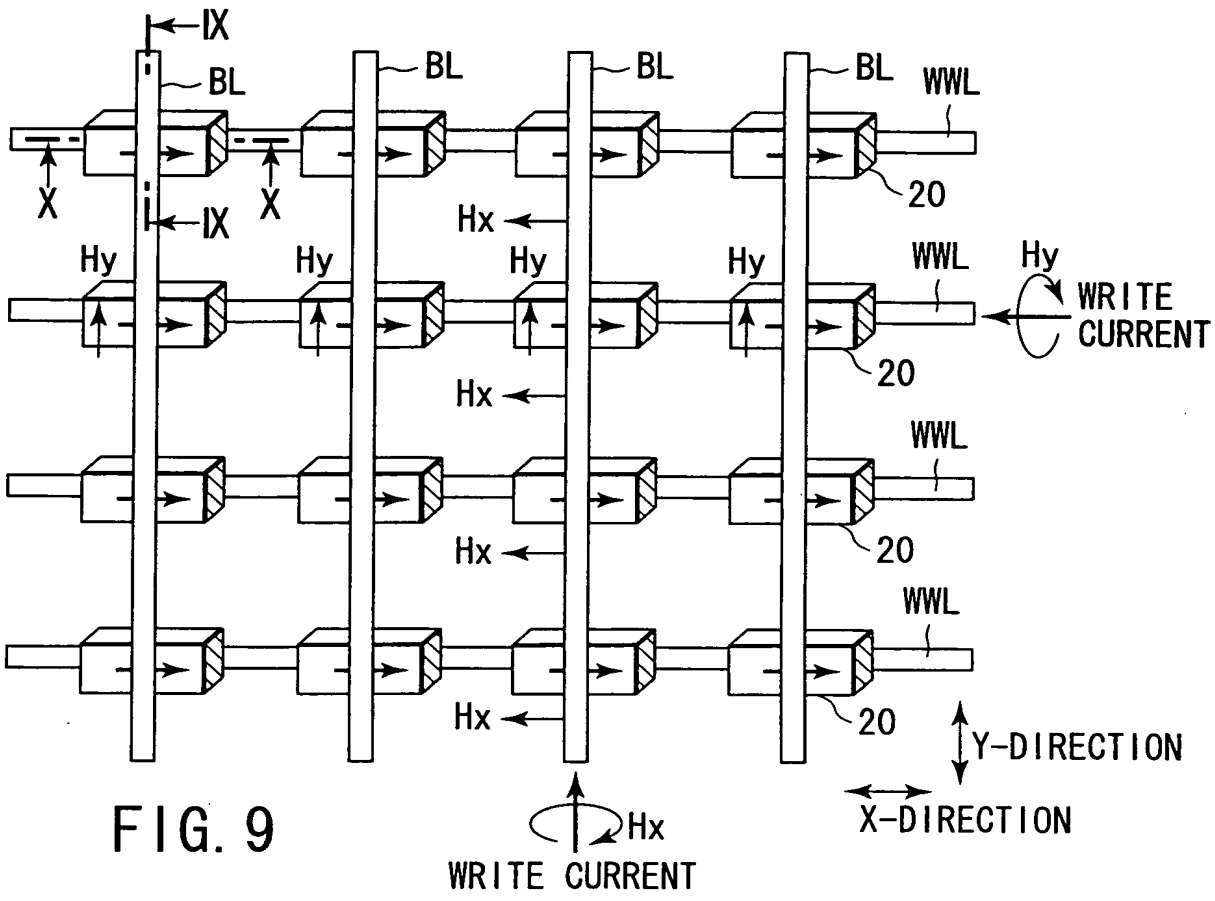


FIG. 9

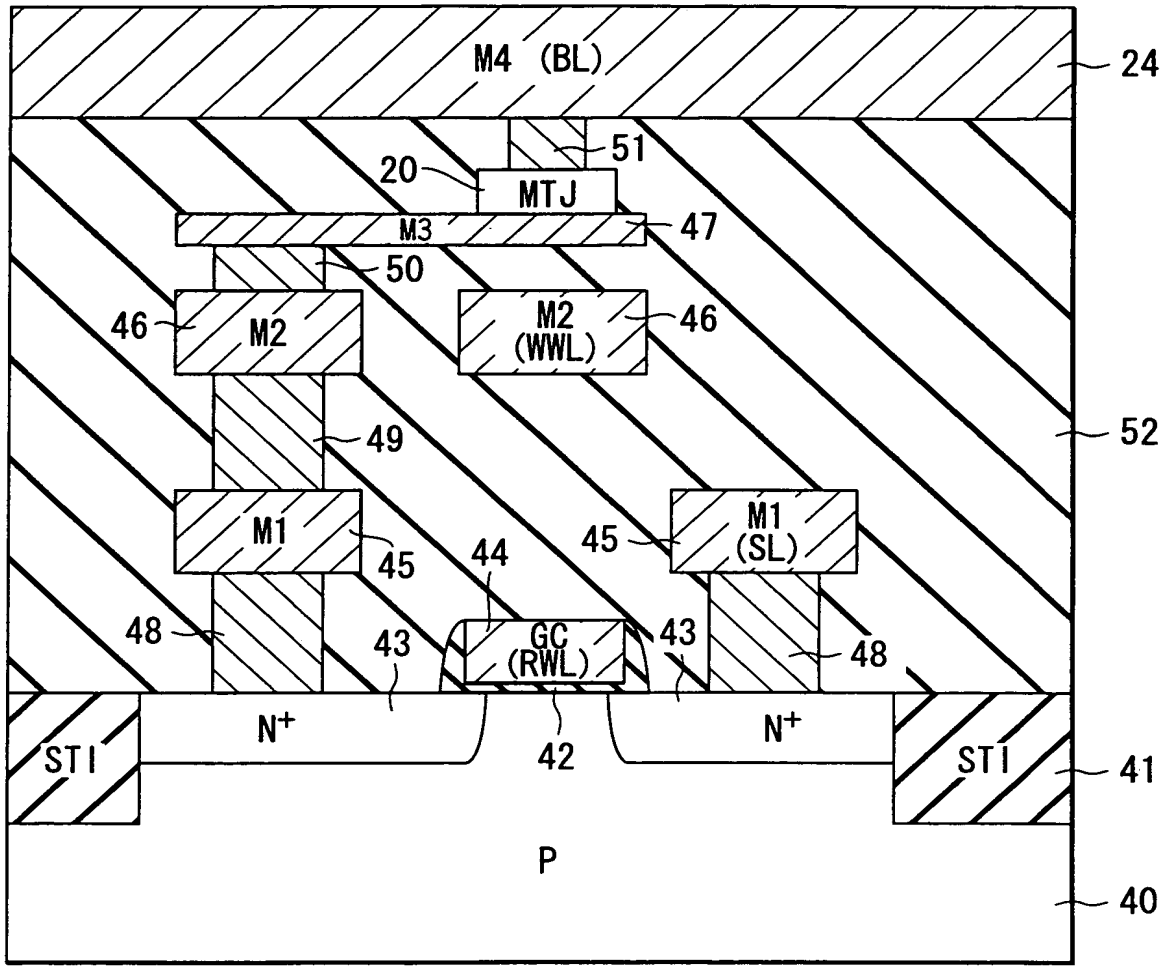

M4 (BL)
24
51
20
MTJ
M3
47
50
46
M2
M2
(WWL)
46
49
52
M1
45
44
45
M1
(SL)
48
43
GC
(RWL)
43
48
N+
42
N+
STI
STI
41
P
40

FIG. 10

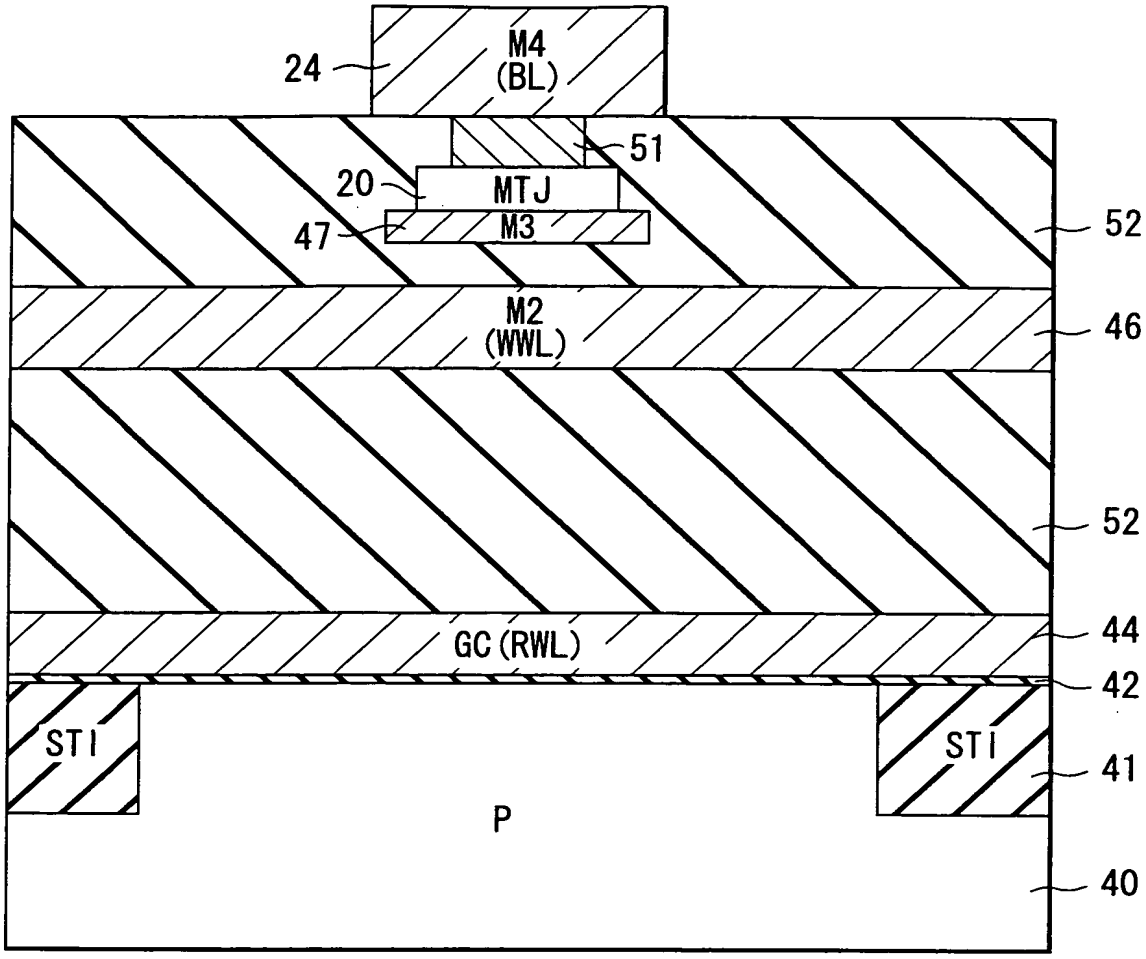

M4
(BL)
24
51
20
MTJ
47
M3
52
M2
(WWL)
46
52
GC (RWL)
44
42
STI
STI
41
P
40

FIG. 11

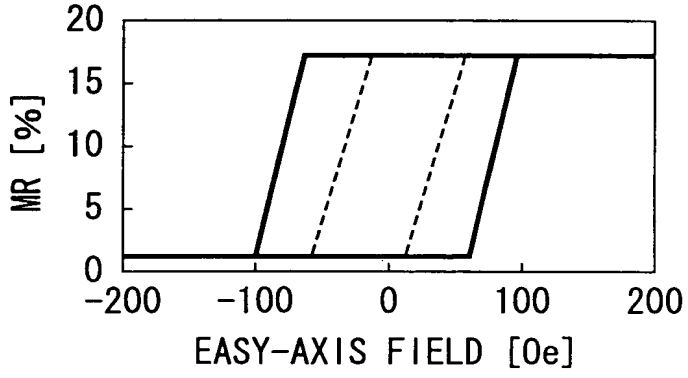

20
15
10
5
0
MR [%]
-200
-100
0
100
200
EASY-AXIS FIELD [Oe]

FIG. 12

FIG. 13

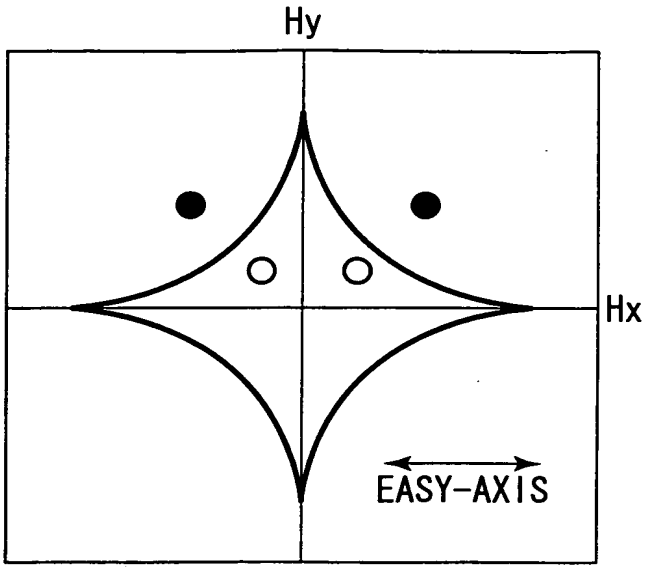


FIG. 14

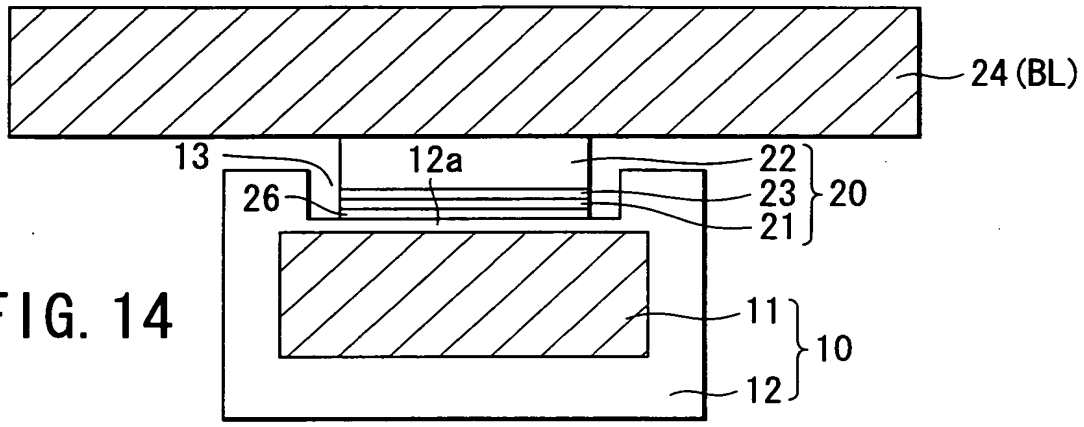


FIG. 15

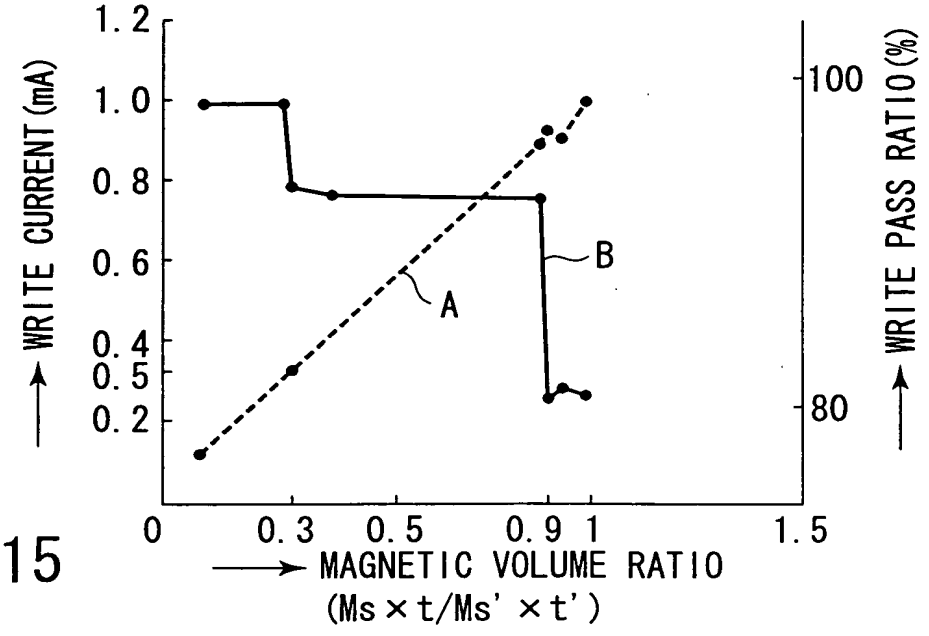


FIG. 16

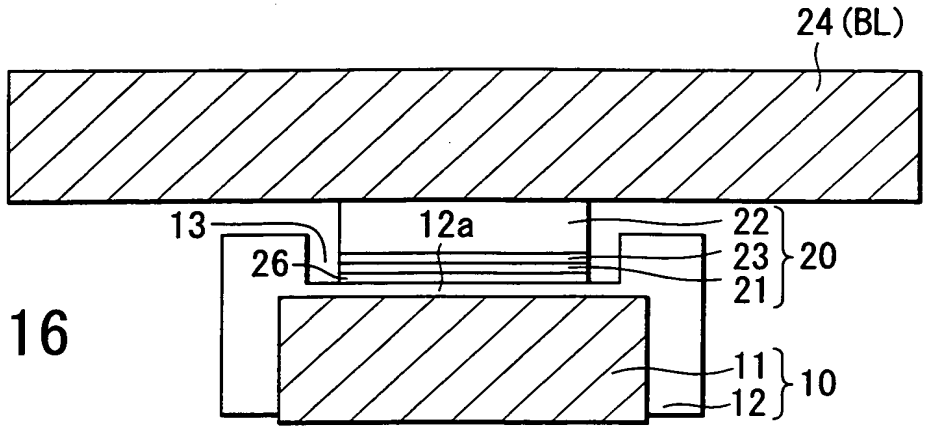


FIG. 17

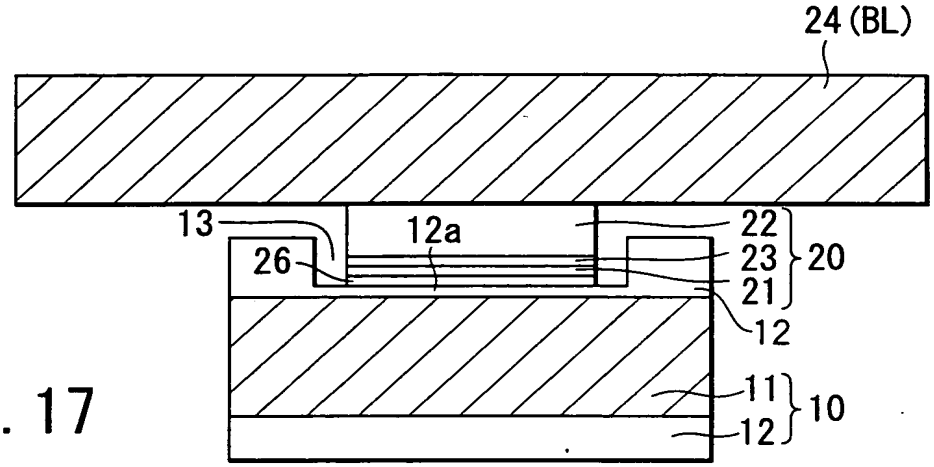
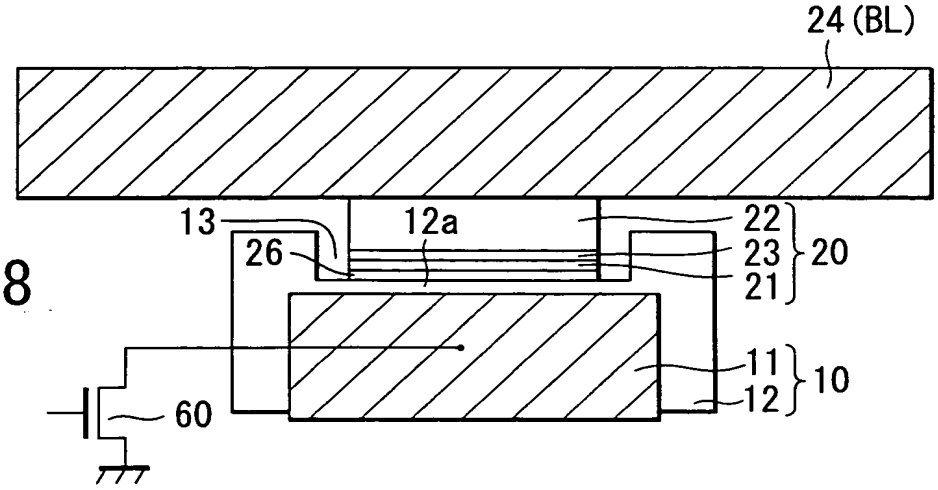


FIG. 18



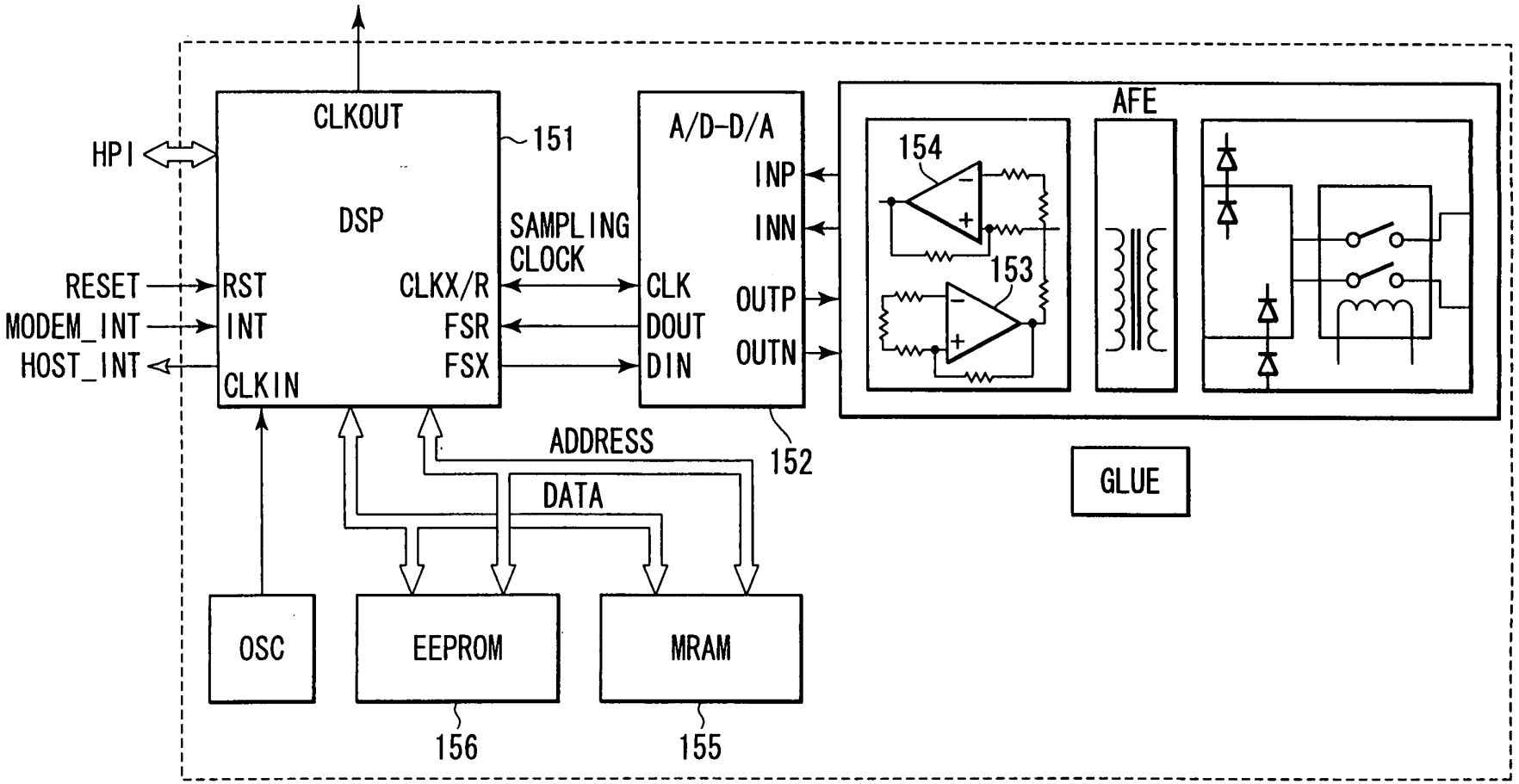

CLKOUT
151
HPI
DSP
SAMPLING
CLOCK
RESET
RST
CLKX/R
MODEM_INT
INT
FSR
HOST_INT
CLKIN
FSX
A/D-D/A
INP
INN
CLK
OUTP
DOUT
OUTN
DIN
154
153
AFE
ADDRESS
152
DATA
GLUE
OSC
EEPROM
MRAM
156
155

FIG. 19

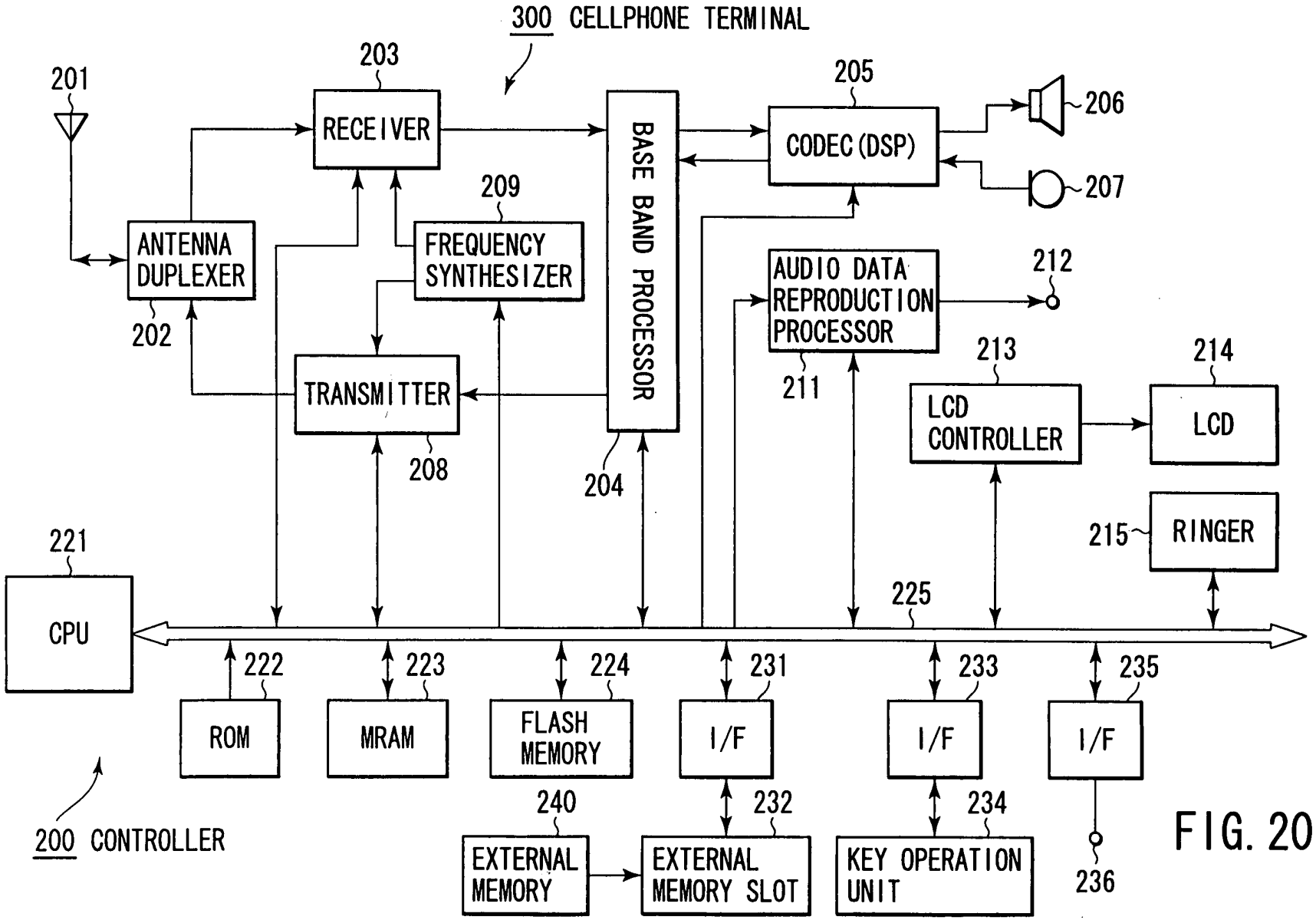

300 CELLPHONE TERMINAL
201
203
RECEIVER
205
CODEC(DSP)
206
207
209
FREQUENCY SYNTHESIZER
BASE BAND PROCESSOR
ANTENNA DUPLEXER
202
AUDIO DATA REPRODUCTION PROCESSOR
212
211
213
LCD CONTROLLER
214
LCD
TRANSMITTER
208
204
215
RINGER
221
CPU
225
222
223
224
231
233
235
ROM
MRAM
FLASH MEMORY
I/F
I/F
I/F
240
232
234
200 CONTROLLER
EXTERNAL MEMORY
EXTERNAL MEMORY SLOT
KEY OPERATION UNIT
236

FIG. 20

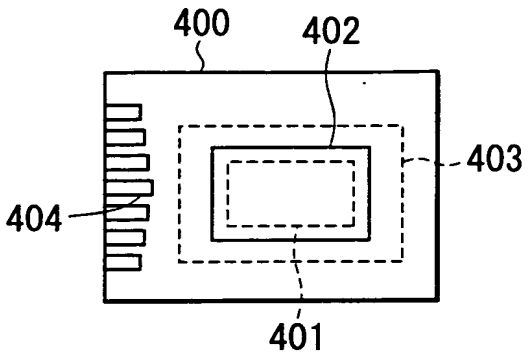


FIG. 21

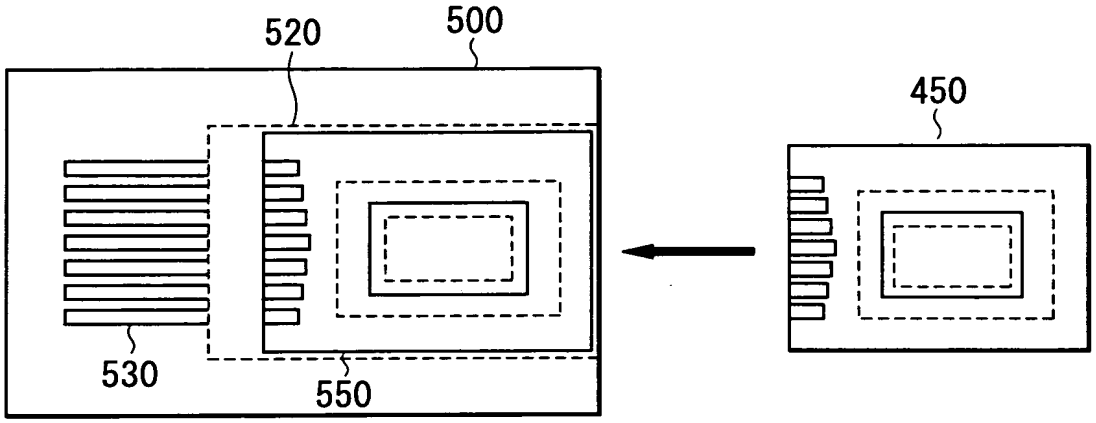
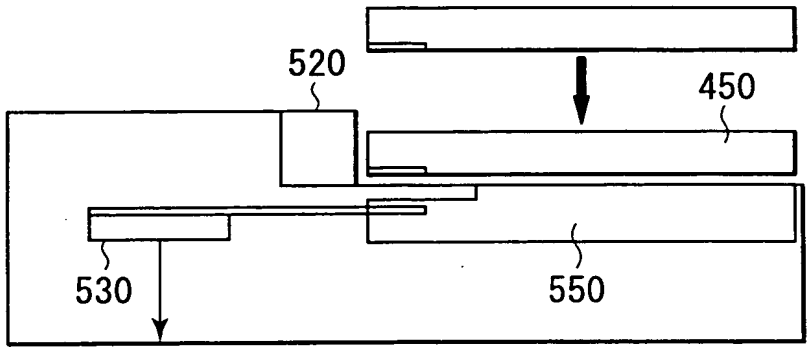


FIG. 22



TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 24

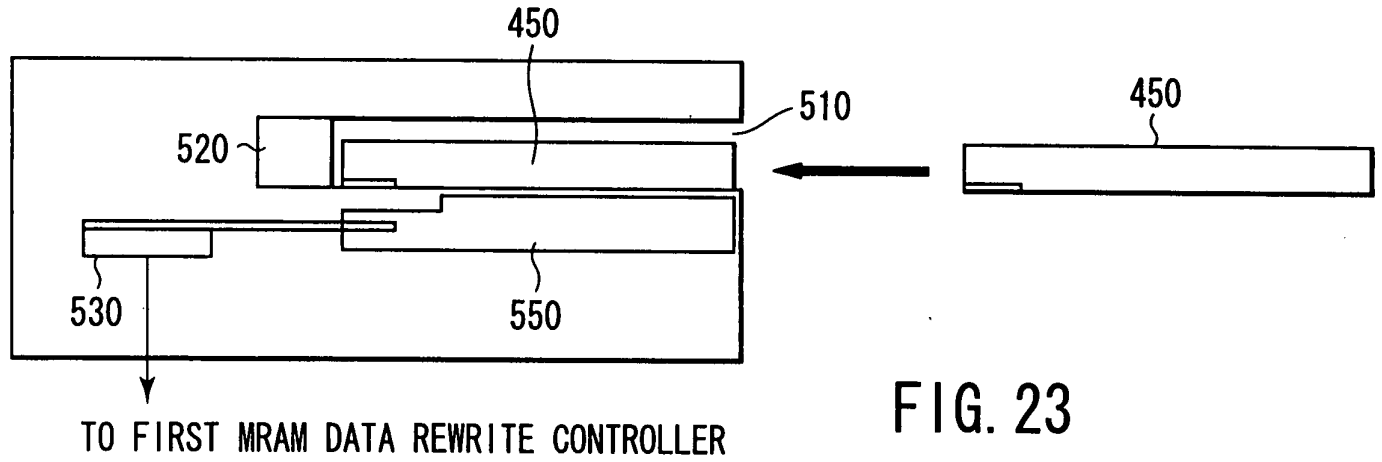

450
510
520
450
530
550
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 23

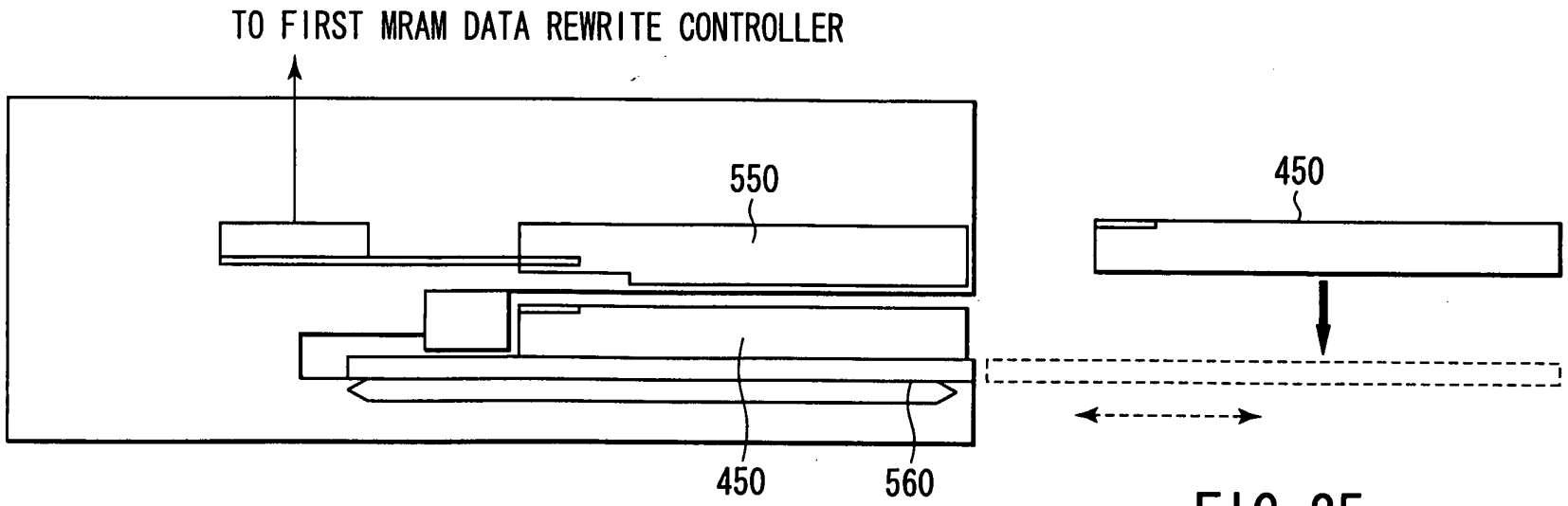

TO FIRST MRAM DATA REWRITE CONTROLLER
550
450
450
560

FIG. 25